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EXAMINER	
PUENTE, EMERSON C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,213	TAI ET AL.	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-20* is/are rejected.

7)☐ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is made **Non-Final.**

Claims 1-20 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 cites in base claim 1 "an SD bus operably connecting the operating system of the platform to the SD host board". Furthermore, claim 3 cites "an SDIO controller reference board equipped with an SDIO port operably connectable to the SDIO host device via the SD bus". However, the specifications discloses the connection between the operating system and SD host board using a different bus than the connection between controller reference board and SDIO host device (see figure 1(b) and paragraph 9 and 11). For examining purposes, examiner interprets claim 3 to merely cite "SDIO controller reference board equipped with an SDIO port operably connectable to the SDIO host device via a connection".

The remaining claims, not specifically mentioned, are rejected because they are dependent upon the claim above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. **103(a)** as being unpatentable over US Patent No. 6,938,244 of Perlin et al. referred hereinafter "Perlin" in view of US Patent No. 6,591,069 of Horiguchi.

In regards to claim 1, Perlin discloses a card development supporting system for development of card, the system comprising:

a hardware component comprising:

(i) a platform having an operating system and a memory operably connected to the operating system (see figure 2 item 102, 138, 140 and column 6 lines 30-53);

(ii) an host board including an host device (see figure 1 item 106, 104 and column 3 lines 52-54); and

(iii) an bus operably connecting the operating system of the platform to the host board (see figure 1 item 108 and column 3 lines 54-59); and

a software component stored in the memory of the platform, wherein the software component comprises an test program that runs on the operating system of the platform. Perlin discloses executable applications including application development tool for debugging a smart card application (see figure 1 item 118 and column 4 lines 39-46).

Perlin further discloses wherein the card is an IC card such as a smart card (see column 2 lines 39-41).

However, Perlin fails to explicitly disclose:

SDIO cards;

Horiguchi discloses smart cards employing memory devices, such as SD cards (see column 1 lines 35-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin and Horiguchi such that the smart cards employee SD cards, indicating SDIO cards. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin discloses using smart cards (see column 2 lines 39-41) that are embedded with a memory device (see column 1 lines 19-20), and SD cards, as per teachings of Horiguchi, constitute suitable memory device for smart cards (see column 1 lines 35-40), indicating SDIO cards. It is further understood since the teachings of Perlin in view of Horiguchi disclose SDIO cards, the card development supporting system would be a SDIO card development supporting system, the host board would be a SD host board, the host device would be a SDIO host device, the bus would be an SD bus, and the test program would be a SDIO test program.

In regards to claim 2, Perlin discloses:

wherein the platform is a computer (see figure 1 item 102 and column 3 lines 47-51).

In regards to claim 3, Perlin discloses:

wherein the hardware component further comprises an controller reference board equipped with an port (see figure 1 item 106 and column 3 lines 52-54) operably connectable to

the SDIO host device via the SD bus (a connection) (see figure 1 item 104 and column 3 lines 52-54). It is further understood since the teachings of Perlin in view of Horiguchi disclose SDIO cards, the controller reference board would be a SDIO controller reference boards and the port would be an SDIO port.

Claims 4 and 5 are rejected under 35 U.S.C. **103(a)** as being unpatentable over Perlin in view of Horiguchi and in further view of US Patent No. 6,407,940 of Aizawa and Microsoft Dictionary referred hereinafter "Microsoft".

In regards to claim 4, Perlin in view of Horiguchi discloses the claim limitations as discussed above. However, Perlin in view of Horiguchi fails to explicitly disclose:

wherein the reference board comprises:

a substrate; an SDIO controller disposed on the substrate and equipped with a plurality of application interfaces; a quartz oscillator operably connected to the SDIO controller; and a plurality of application interface ports operably connected to the SDIO controller.

Aizawa discloses a reference board comprising

a substrate (see figure 1 item 11 and column 3 lines 14-15);

an SDIO controller disposed on the substrate (see figure 1 item 111 and column 3 lines 14-15) and equipped a plurality of application interfaces (see figure 1 items 201,203 and column 3 lines 22-25);

a oscillator operably connected to the SDIO controller (see figure 2 item 401 and column 5 lines 52-53); and

a plurality of application interface ports operably connected to the SDIO controller (see figure 1 items 201,203 and column 3 lines 22-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Horiguchi, and Aizawa such that the reference board comprises a substrate, an SDIO controller disposed on the substrate and equipped with a plurality of application interfaces, a quartz oscillator operably connected to the SDIO controller, and a plurality of application interface ports operably connected to the SDIO controller. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin in view of Horiguchi discloses a smart card employing SD card (see column 1 lines 35-40 of Horiguchi) and a substrate, an SDIO controller disposed on the substrate and equipped with a plurality of application interfaces, a quartz oscillator operably connected to the SDIO controller, and a plurality of application interface ports operably connected to the SDIO controller (see figure 1 and 2; column 3 lines 1-25 and column 5 lines 52-53), as per teachings of Aiwaza, constitutes known components of an SD card.

Microsoft further discloses:

quartz crystal are used by oscillator circuits to generate a stable frequency (see page 324 term "oscillator").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Horiguchi, Aizawa, and Microsoft to use a quartz oscillator. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Aizawa discloses an oscillator (see figure 2 item 401 and column 5 lines 52-53), and as such, is concerned with providing a periodically varying

output at a controlled frequency, and a quartz oscillator, as per teachings of Microsoft, constitute a known type of oscillator capable of providing a stable frequency (see page 324 term "oscillator").

In regards to claim 5, Aizawa further discloses:

wherein the SDIO controller further comprises a host interface module that operably connects the SDIO controller to the SD bus when the SDIO port is operably connected to the SDIO host device (see figure 1 item 201 and column 3 lines 28-30).

Claim 7 is rejected under 35 U.S.C. **103(a)** as being unpatentable over Perlin in view of Horiguchi and in further view of US Patent No. 6,826,747 of Augsburg et al. referred hereinafter "Augsburg".

In regards to claim 7, Perlin in view of Horiguchi discloses the claim limitations as discussed above. Perlin further discloses generate commands and perform debugging for the SD host device (see column 11 lines 1-20).

However, Perlin in view of Horiguchi fails to explicitly disclose:

wherein the SDIO test program operates to analyze commands and trace commands.

Augsburg discloses during debugging, it is known for users to trace instructions (commands), as well as analyze the trace in order to determine the performance of the program or application (see column 1 lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Horiguchi, and Augsburg to trace instructions, as well as analyze the trace in order to determine the performance of the program, indicating the

SDIO test program operates to analyze commands and trace commands. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with debugging (see column 11 lines 1-5) and Augsburg discloses during debugging, it is known for users to trace instructions (commands), as well as analyze the trace in order to determine the performance of the program (see column 1 lines 25-30).

Claims 8 and 9 are rejected under 35 U.S.C. **103(a)** as being unpatentable over Perlin in view of Horiguchi and in view of Augsburg and in further view of US Patent No. 6,993,748 of Schaefer.

In regards to claim 8, Perlin in view of Horiguchi and Augsburg discloses the claim limitations as discussed above. However, Perlin in view of Horiguchi and Augsburg fails to explicitly disclose:

wherein the SDIO test program also operates a language script interpreter in order to describe generated commands, analyzed commands, traced commands, and debugging performed by the SDIO test program.

Schaefer disclose testing/debugging an application or software program via test scripts (see column 1 lines 15-19 and 55-60). Schaefer further discloses an interpreter for executing the test scripts (see column 1 lines 62-65), indicating language script interpreter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Horiguchi, Augsburg, and Schaefer such that the debugging is executed using test script. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with

testing/debugging applications (see column 3 lines 47-50) and using test scripts, as per teachings of Schaefer, constitute a known means of testing/debugging an application that enable automated testing/debugging of the applications (see column 1 lines 15-19). Since debugging using test scripts would require an interpreter for executing the test script (see column 1 lines 62-65 of Schaefer), the combination would teach the language script interpreter.

In regards to claim 9, Perlin in view of Horiguchi discloses the claim limitations as discussed above. However, Perlin further discloses:

wherein the SDIO test program comprises a command generator (see column 11 lines 38-40).

However, Perlin in view of Horiguchi fails to explicitly disclose:

a command analyzer, a tracer, and a language script interpreter.

Augsburg discloses during debugging, it is known for users to trace instructions (commands), as well as analyze the trace in order to determine the performance of the program (see column 1 lines 25-30), indicating a command analyzer and a tracer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Horiguchi, and Augsburg to trace instructions, as well as analyze the trace in order to determine the performance of the program, indicating indicating a command analyzer and a tracer. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with debugging (see column 11 lines 1-5) and Augsburg discloses during debugging, it is known for users to trace instructions (commands), as well as analyze the trace in order to determine the performance of the program (see column 1 lines 25-30).

Furthermore, Schaefer discloses testing/debugging an application or software program via test scripts (see column 1 lines 15-19 and 55-60). Schaefer further discloses an interpreter for executing the test scripts (see column 1 lines 62-65), indicating language script interpreter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Horiguchi, Augsburg, and Schaefer such that the debugging is executed using test script. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with testing/debugging applications (see column 3 lines 47-50) and using test scripts, as per teachings of Schaefer, constitute known means of testing/debugging an application that enable automated testing/debugging of the applications (see column 1 lines 15-19). Since debugging using test scripts would require an interpreter for executing the test script (see column 1 lines 62-65 of Schaefer), the combination would teach the language script interpreter.

Claims 10-12 and 14 are rejected under 35 U.S.C. **103(a)** as being unpatentable over Aizawa in view of Microsoft.

In regards to claim 10, Aizawa discloses an SDIO controller reference board (see figure 1 item 11 and column 3 lines 14-15) equipped with an SDIO port operably connectable to an SDIO host device via an SD bus (see figure 1 item 12 and column 3 lines 16-18), the reference board comprising:

(a) a substrate (see figure 1 item 11 and column 3 lines 14-15);

(b) an SDIO controller disposed on the substrate (see figure 1 item 111 and column 3 lines 14-15) and having a plurality of application interfaces (see figure 1 items 201,203 and column 3 lines 22-25);

(c) a oscillator operably connected to the SDIO controller (see figure 2 item 401 and column 5 lines 52-53); and

(d) a plurality of application interface ports operably connected to the SDIO controller (see figure 1 items 201,203 and column 3 lines 22-25).

However, Aizawa fails to explicitly disclose:

a quartz oscillator;

Microsoft discloses:

quartz crystal are used by oscillator circuits to generate a stable frequency (see page 324 term "oscillator").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Aizawa and Microsoft to use a quartz oscillator. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Aizawa discloses an oscillator (see figure 2 item 401 and column 5 lines 52-53), and as such, is concerned with providing a periodically varying output at a controlled frequency, and a quartz oscillator, as per teachings of Microsoft, constitute a known type of oscillator capable of providing a stable frequency (see page 324 term "oscillator").

In regards to claim 11, Aizawa discloses:

wherein the SDIO controller further comprises a host interface module that operably connects the SDIO controller to the SD bus when the SDIO port is operably connected to the SDIO host device (see figure 1 item 201 and column 3 lines 28-30) .

In regards to claim 12, Aizawa discloses:

wherein the SDIO controller further comprises a memory interface (see figure 1 item 203 and column 3 lines 22-25), and the reference board further comprises one or more memory units operably connected to the memory interface (see figure 1 item 112 and column 3 lines 14-15).

In regards to claim 14, Aizawa discloses:

wherein each application interface of the SDIO controller is operably connected to a respective one of the plurality of application interface ports (see figure 1 items 201,203 and column 3 lines 22-25);

Claim 13 is rejected under 35 U.S.C. **103(a)** as being unpatentable over Aizawa in view of Microsoft and in further view of US Patent 6,820,047 of Aizawa et al. referred hereinafter "Aizawa 2".

In regards to claim 13, Aizawa in view of Microsoft discloses the claim limitations as discussed above. Aizawa further discloses writing data onto a memory core comprising of Flash EEPROM (see figure 1 item 112 and column 3 lines 15-21).

However, Aizawa in view of Microsoft fails to explicitly disclose:

wherein the one or more memory units are selected from the group consisting of an I^2C serial EEPROM unit, a NAND-type flash memory and a NOR-type flash memory.

Aizawa 2 discloses NAND type flash EEPROM as a known type of flash memory (see column 3 lines 54-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Aizawa, Microsoft, and Aizawa 2 to use a NAND type flash EEPROM, thus indicating a NAND-type flash memory. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Aizawa is concerned with writing data onto a memory core comprising of Flash EEPROM (see figure 1 item 112 and column 3 lines 15-21) and a NAND-type flash EEPROM memory, as per teachings of Aizawa 2, constitutes a known type of Flash EEPROM providing storage of data (see column 3 lines 54-56).

Claims 16 and 17 are rejected under 35 U.S.C. **103(a)** as being unpatentable over Perlin in view of US Patent No. 6,615,390 of Takagi and Horiguchi.

In regards to claim 16, Perlin discloses a card development supporting system, wherein the system comprises an integrated development environment software program operating on a computer platform (see figure 1) comprising a memory storing the software program (see figure 2 item 134) and host device (see figure 1 item 102), the method comprising the steps of:

(a) starting the card development supporting system using the software program and optionally checking a work environment (see figure 1 and column 3 lines 47-52);

(b) launching one or more engines of the software program. Perlin discloses invoking the debug environment, which can be a stand alone application (see column 11 lines 32-37);

(c) initializing the system using the software program when an card unit having an controller is inserted into an slot of the computer platform so as to operably connect the controller to the host device. Perlin discloses connecting a card, which includes a development interface, to a computer system (see figure 1 item 110 and column 3 lines 48-52). The development interface includes control logic, which can be a controller (see figure 5 item 502 and column 9 lines 42-46).

However, Perlin fails to explicitly disclose:

generating an SDIO command using the software program in order to test the operable connection between the SDIO host device and SDIO controller.

SDIO cards;

Takagi discloses a tester starting a session with an IC card and determining whether there is error when establishing a session (connection) with the IC card (see column 9 lines 8-10), indicating generating an command using the software program in order to test the operable connection between the host device and controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin and Takagi to determine whether there is error when establishing a session (connection) with the IC card, thus indicating generating an command using the software program in order to test the operable connection between the host device and controller. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with establishing a connection or session with an IC card (see figure 1 column 3 lines 48-54 and column 4 lines 16-

17), and testing the operable connection, as per teachings of Takagi, verifies there are no fault or error in the connection with the IC card (see column 9 lines 8-10).

Horiguchi further discloses smart cards employing memory devices, such as SD cards (see column 1 lines 35-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Takagi and Horiguchi such that the smart cards employee SD cards, indicating SDIO cards. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin discloses using smart cards (see column 2 lines 39-41) that are embedded with a memory device (see column 1 lines 19-20), and SD cards, as per teachings of Horiguchi, constitute suitable memory device for smart cards (see column 1 lines 35-40), indicating SDIO cards. It is further understood since the teachings of combine teachings of Perlin, Takagi, Horiguchi disclose SDIO cards, the card development supporting system would be a SDIO card development supporting system, the software program would be an SD software program, the host device would be a SDIO host device, the controller would be an SDIO controller, the test program would be a SDIO test program, and the command would be an SDIO command.

In regards to claim 17, Perlin further discloses:

wherein the software program comprises an SDIO initialization engine and an SDIO command process engine, and initializing of the system is performed by the SDIO initialization engine and generating the SDIO command is performed by the SDIO command process engine. Perlin discloses invoking the debug environment of the host computer (see column 11 lines 32-37), indicating a SDIO initialization engine initializing of the system, and invoking a debug

feature which generates a debug command (see column 11 lines 38-41), indicating SDIO command process engine generating the SDIO command.

Claim 18 is rejected under 35 U.S.C. **103(a)** as being unpatentable over Perlin in view of Takagi and Horiguchi and in further view of US Patent No. 6,466,007 of Prazeres da Costas et al. referred hereinafter "Prazeres da Costa".

In regards to claim 18, Perlin in view of Takagi and Horiguchi discloses the claim limitations as discussed above. However Perlin in view of Takagi and Horiguchi fails to explicitly disclose:

comparing behavior of the SDIO controller of the SDIO card unit to behavior of an ideal SDIO controller stored in memory of the computer platform and generating an error signal when a difference between the behavior of the SDIO controller of the SDIO card unit and the behavior of the ideal SDIO controller is detected.

Prazeres da Costa discloses testing smart cards (see column 3 lines 24-25) and indicating whether a device being tested has failed by comparing the expected results with actual results (see column 4 lines 43-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Takagi, Horiguchi, and Prazeres da Costa to indicate whether a device being tested has failed by comparing the expected results with actual results, thus indicating comparing behavior of the SDIO controller of the SDIO card unit to behavior of an ideal SDIO controller stored in memory of the computer platform and generating an error signal when a difference between the behavior of the SDIO controller of the SDIO card

unit and the behavior of the ideal SDIO controller is detected. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin discloses debugging or testing a smart card (see column 3 lines 47-50), and as such, is concerned with determining whether the smart card is faulty, and comparing the expected results with actual results, as per teachings of Prazeres da Costa, enables testing smart cards to detect faulty ones (see column 4 lines 43-46).

Claims 19 and 20 are rejected under 35 U.S.C. **103(a)** as being unpatentable over Perlin in view of Takagi and Horiguchi and in further view of Augsburg.

In regards to claim 19, Perlin in view of Takagi and Horiguchi discloses the claim limitations as discussed above. Perlin further discloses the operable connection between the SDIO host device and the SDIO controller is provided by an SD bus of the computer platform (see figure 1 item 108 and column 3 lines 54-59).

However, Perlin in view of Takagi and Horiguchi fails to explicitly disclose:

recording a transaction history of packets supported by the bus and parsing and analyzing the transaction history in order to debug the software program when the SDIO card unit is a SDIO controller reference board.

Augsburg discloses during debugging, it is known for users to trace instructions, as well as analyze the trace in order to determine the performance of the program or application (see column 1 lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Takagi, Horiguchi, and Augsburg to trace

instructions, as well as analyze the trace in order to determine the performance of the program, indicating recording a transaction history of packets supported by the bus and parsing and analyzing the transaction history in order to debug the software program when the SDIO card unit is a SDIO controller reference board. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with debugging (see column 11 lines 1-5) and Augsburg discloses during debugging, it is known for users to trace instructions (commands), as well as analyze the trace in order to determine the performance of the program (see column 1 lines 25-30).

In regards to claim 20, Perlin in view of Takagi and Horiguchi discloses the claim limitations as discussed above. Perlin further discloses the operable connection between the SDIO host device and the SDIO controller is provided by an SD bus of the computer platform (see figure 1 item 108 and column 3 lines 54-59).

However Perlin in view of Takagi and Horiguchi fails to explicitly disclose:

recording a transaction history of packets supported by the bus and parsing and analyzing the transaction history in order to debug the software program when the SDIO card unit is an actual SDIO card.

Augsburg discloses during debugging, it is known for users to trace instructions, as well as analyze the trace in order to determine the performance of the program or application (see column 1 lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Perlin, Takagi, Horiguchi, and Augsburg to trace instructions, as well as analyze the trace in order to determine the performance of the program,

indicating recording a transaction history of packets supported by the bus and parsing and analyzing the transaction history in order to debug the software program when the SDIO card unit is an actual SDIO card. A person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings because Perlin is concerned with debugging (see column 11 lines 1-5) and Augsburg discloses during debugging, it is known for users to trace instructions (commands), as well as analyze the trace in order to determine the performance of the program (see column 1 lines 25-30).

Allowable Subject Matter

Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emerson Puente

Emerson Puente
Examiner
AU 2113